



Inventor: MUNNS
Docket No.: 3165.41USU1
Title: SUPER LATTICE MODIFICATION OF OVERLYING TRANSISTOR
Serial No.: 10/723,382
Sheet 1 of 15

FIG.1A

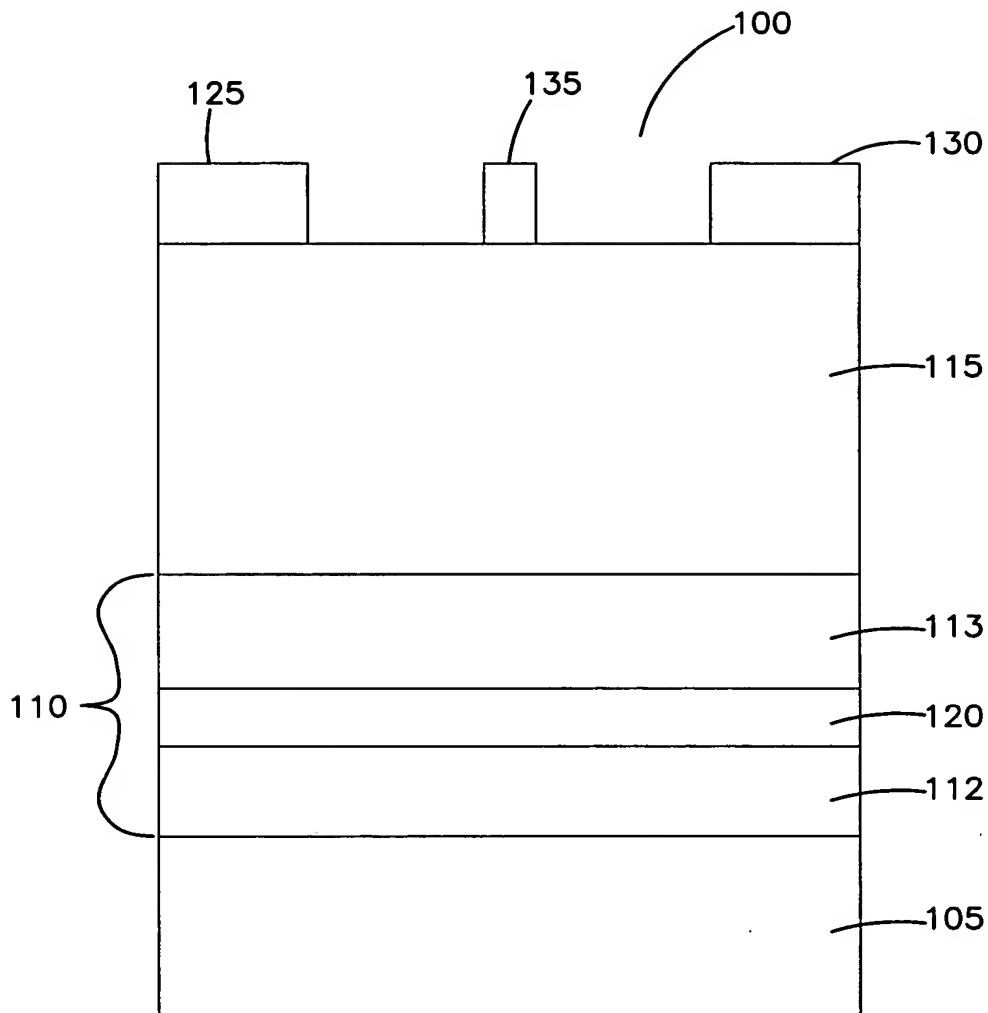




FIG.1B

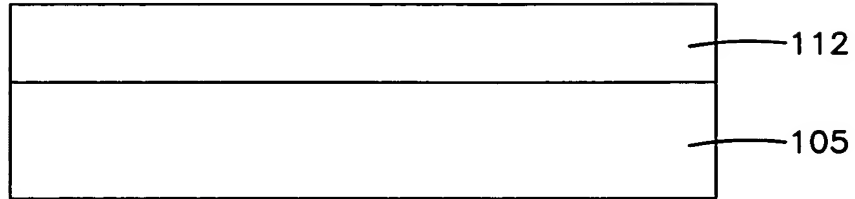


FIG.1C

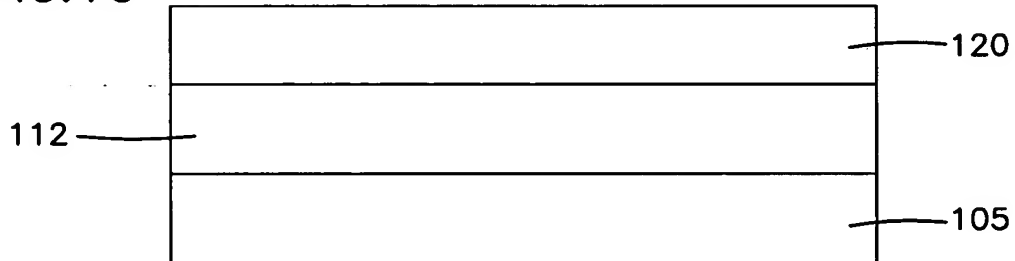


FIG.1D

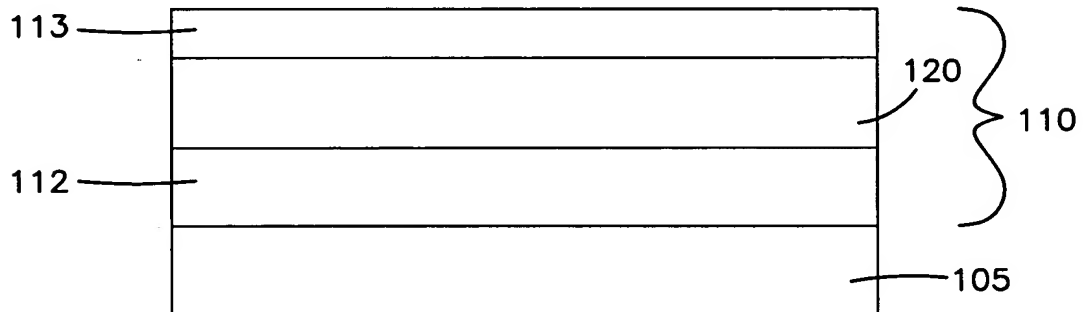


FIG.1E

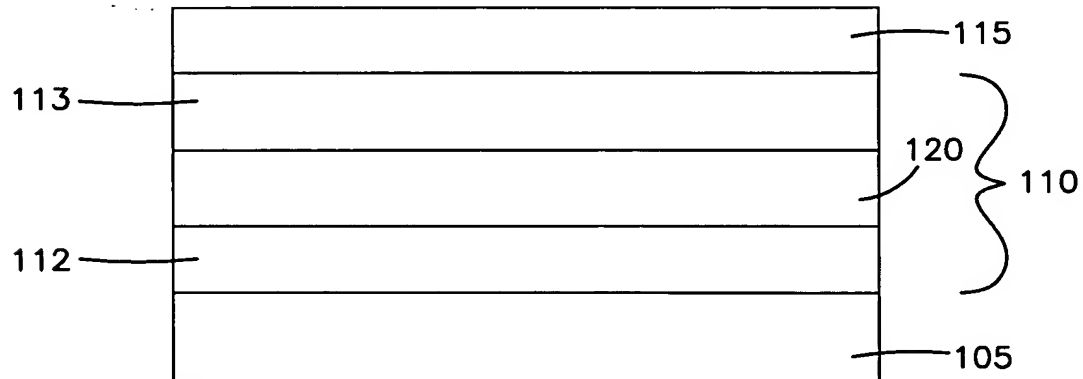




FIG.1F

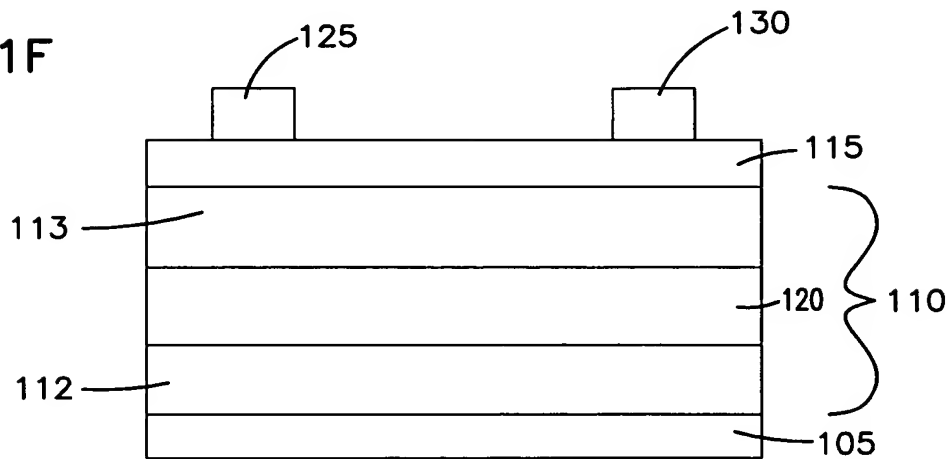


FIG.1G

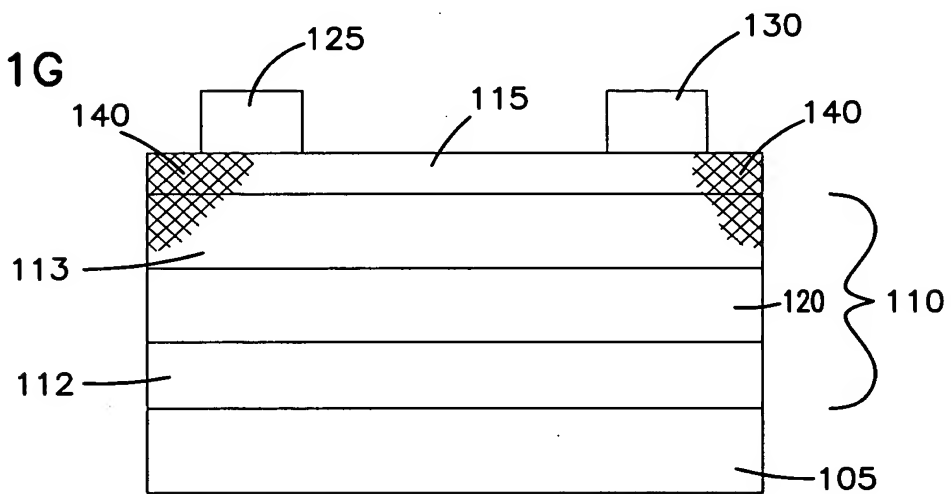


FIG.1H

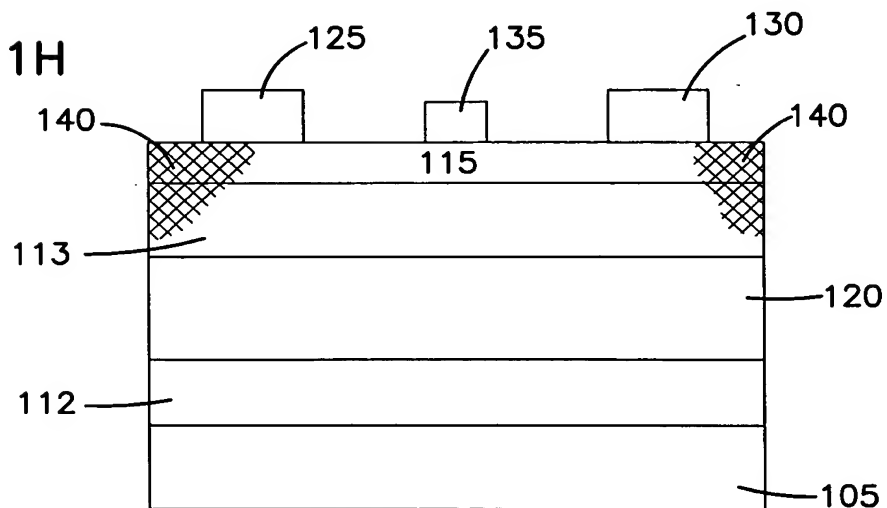




FIG.2

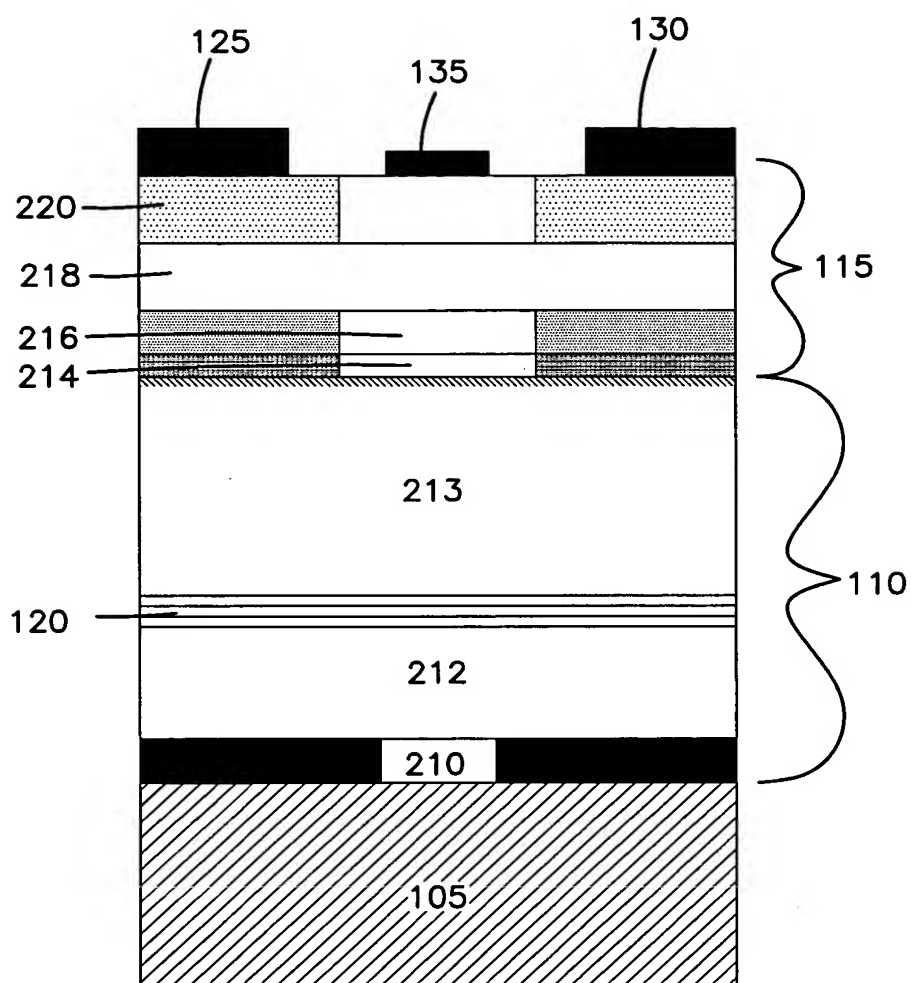




FIG.3

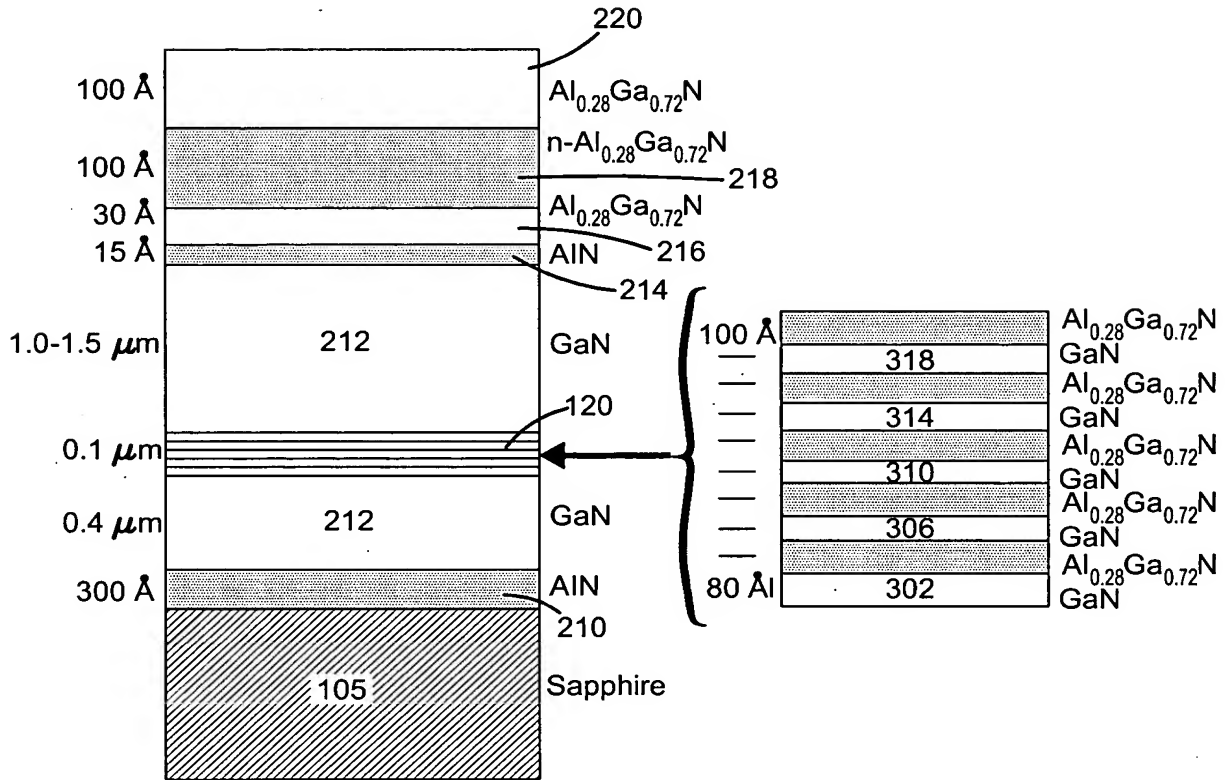
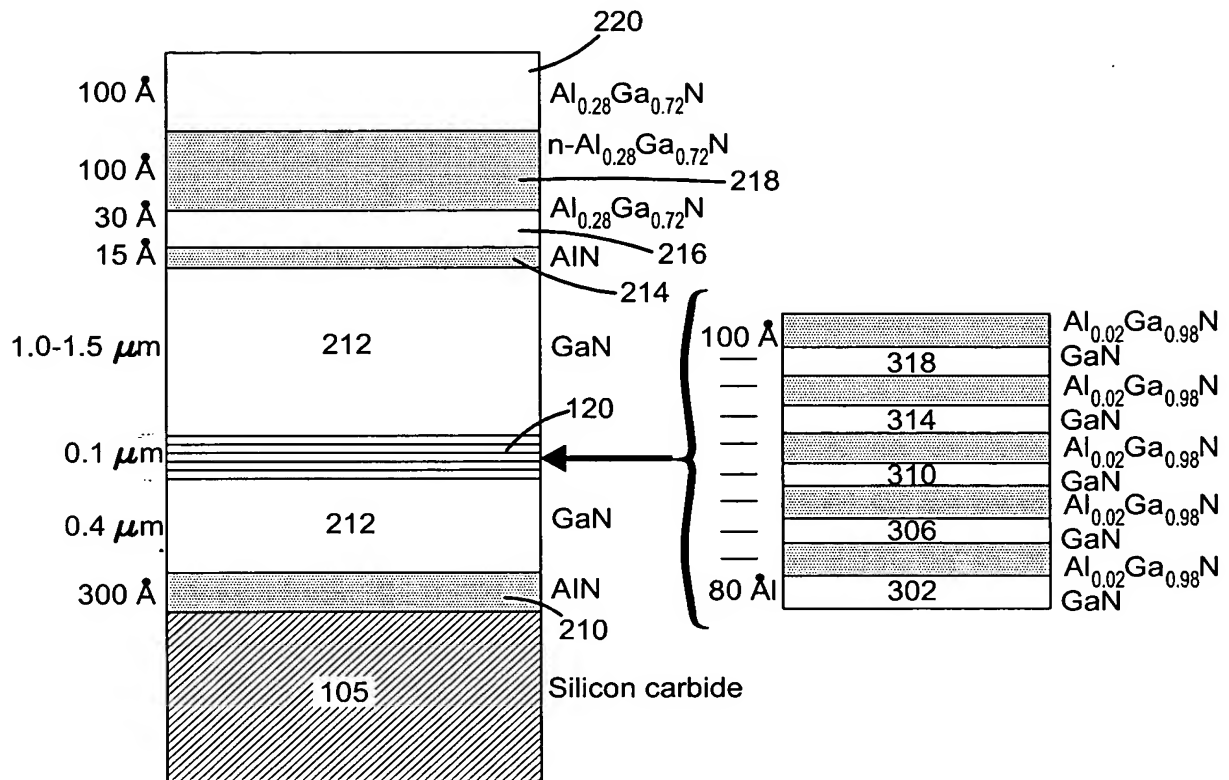




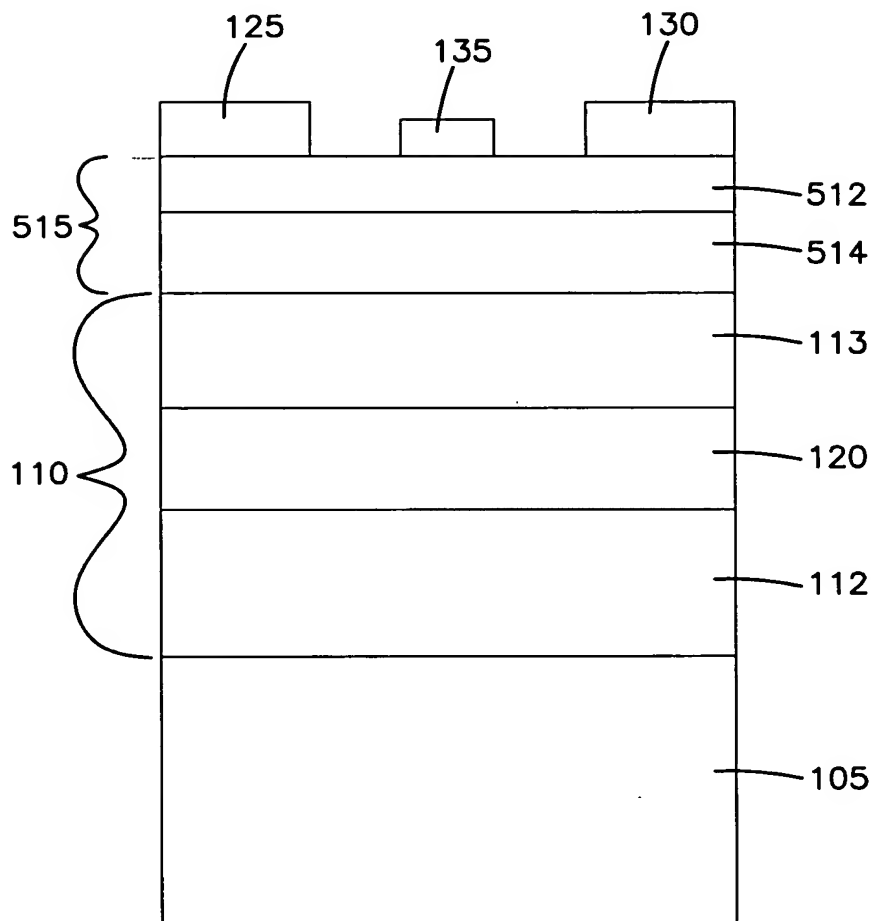
FIG.4





Inventor: MUNNS
Docket No.: 3165.41USU1
Title: SUPER LATTICE MODIFICATION OF OVERLYING TRANSISTOR
Serial No.: 10/723,382
Sheet 7 of 15

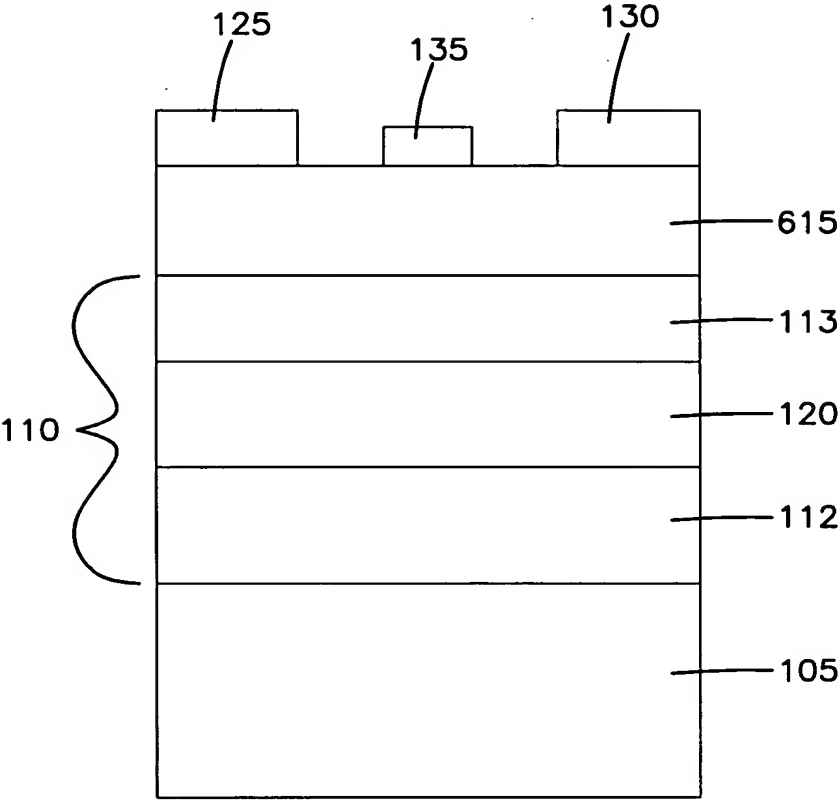
FIG.5





Inventor: MUNNS
Docket No.: 3165,41USU1
Title: SUPER LATTICE MODIFICATION OF OVERLYING TRANSISTOR
Serial No.: 10/723,382
Sheet 8 of 15

FIG.6





Inventor: MUNNS
Docket No.: 3165,41USU1
Title: SUPER LATTICE MODIFICATION OF OVERLYING TRANSISTOR
Serial No.: 10/723,382
Sheet 9 of 15

FIG. 7

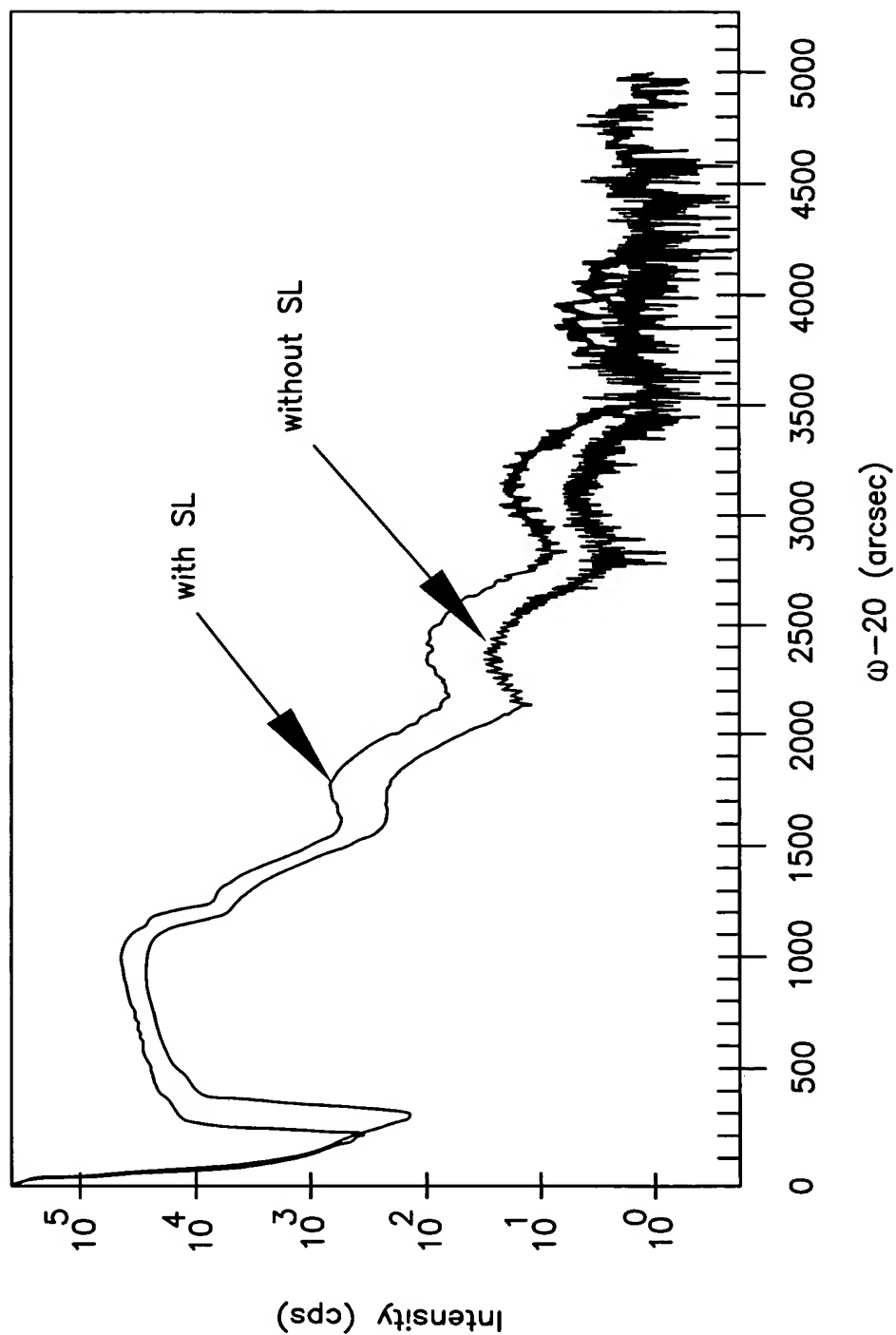




FIG. 8A

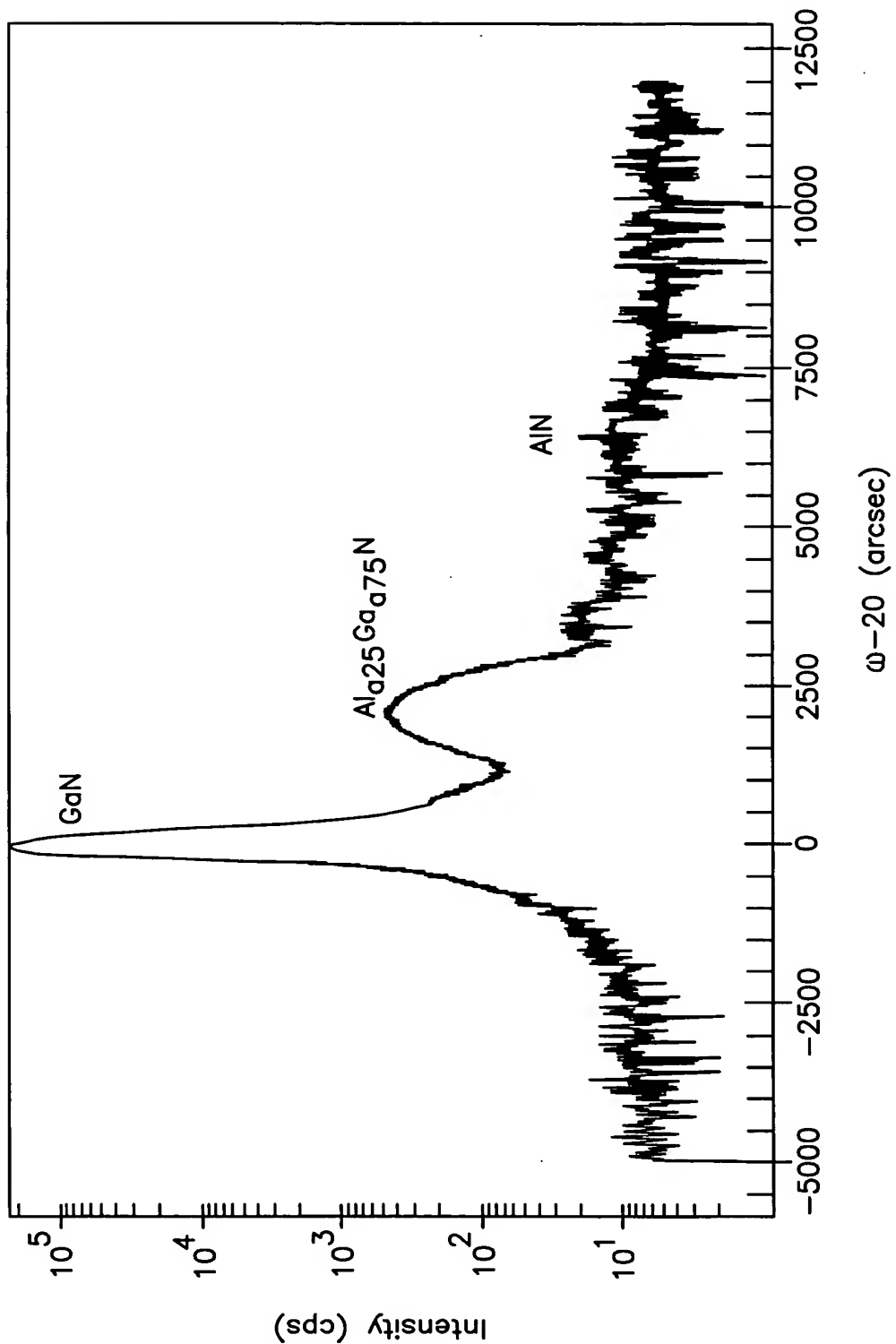




FIG. 8B

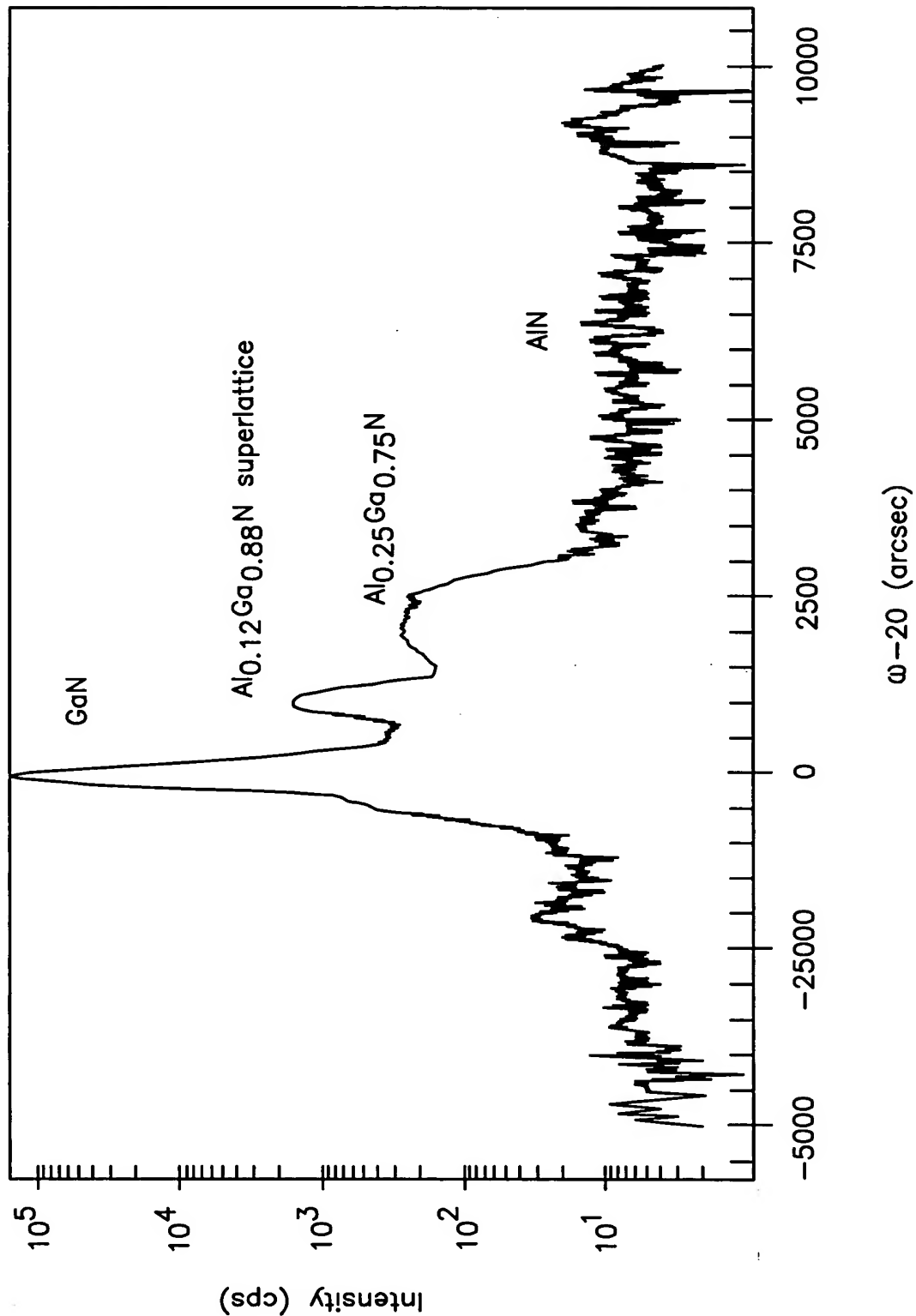




FIG. 9

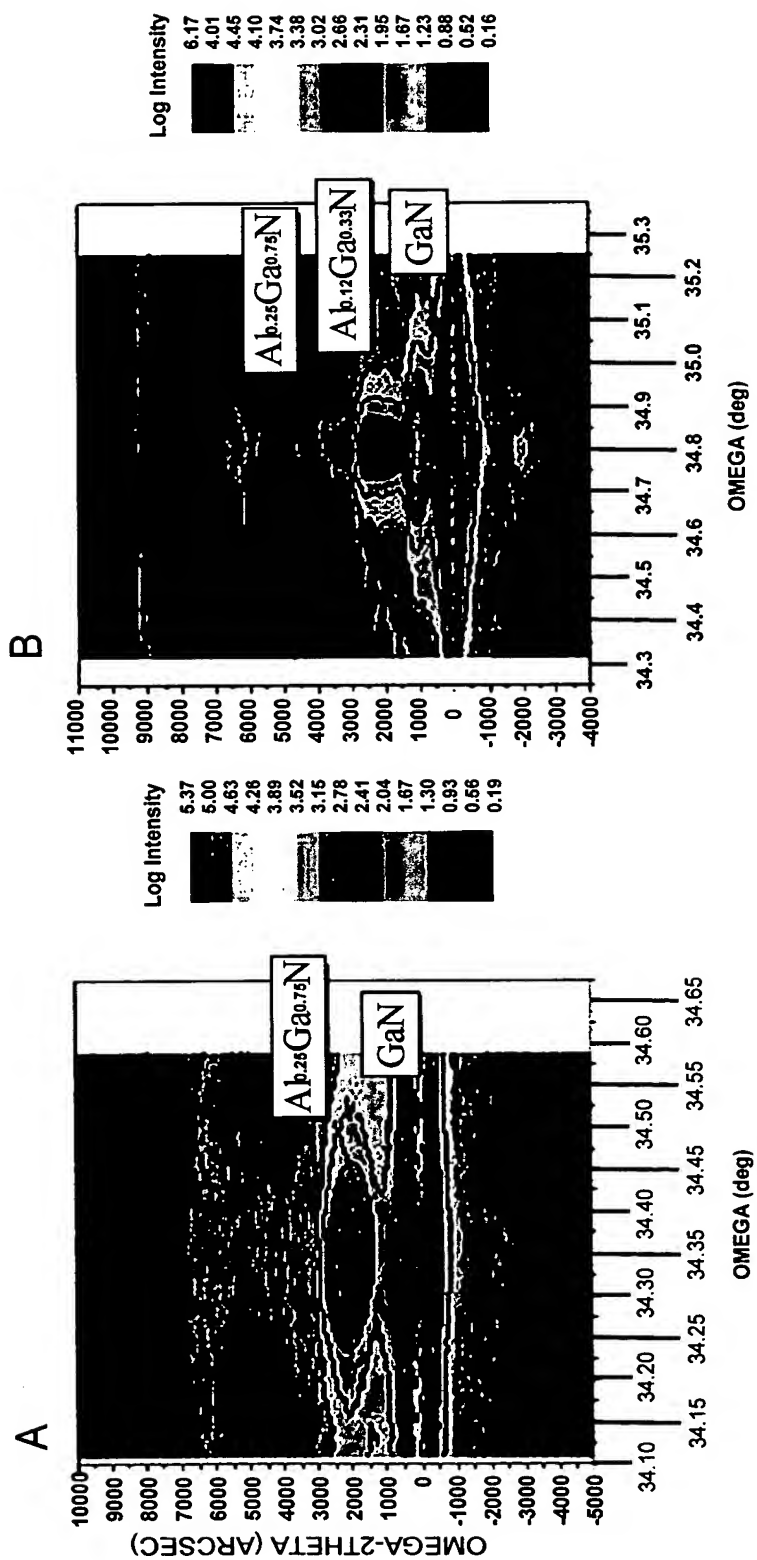
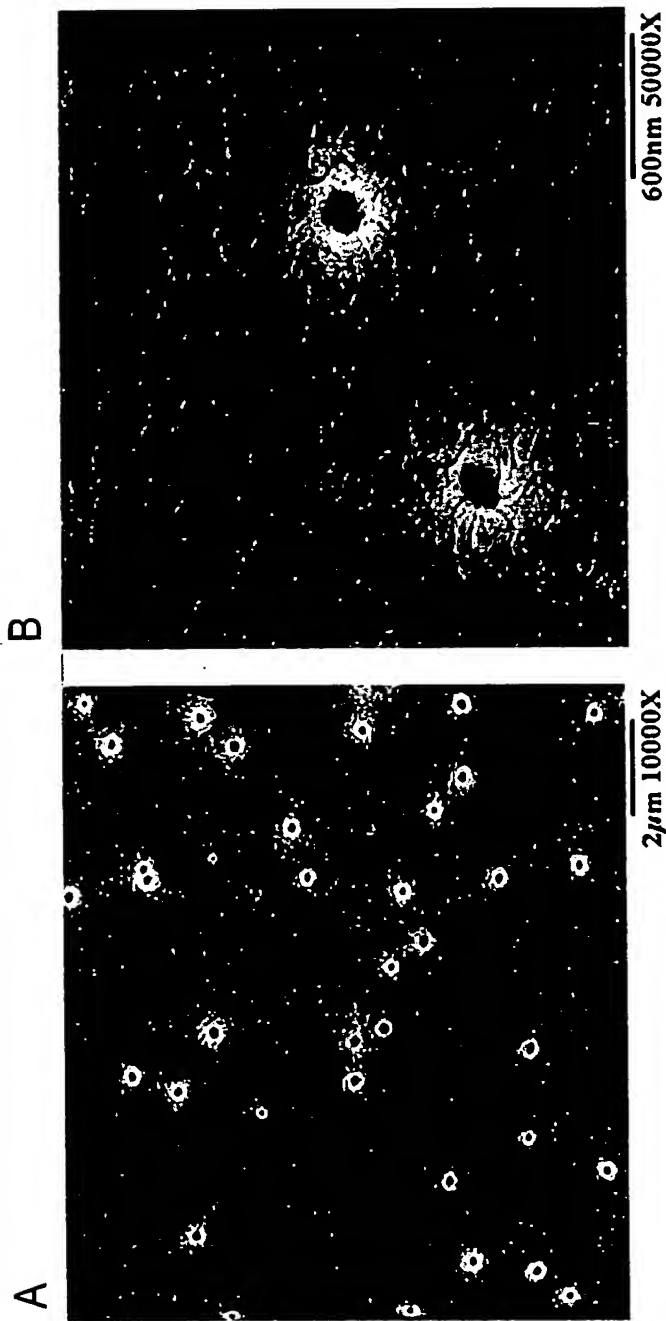




FIG. 10



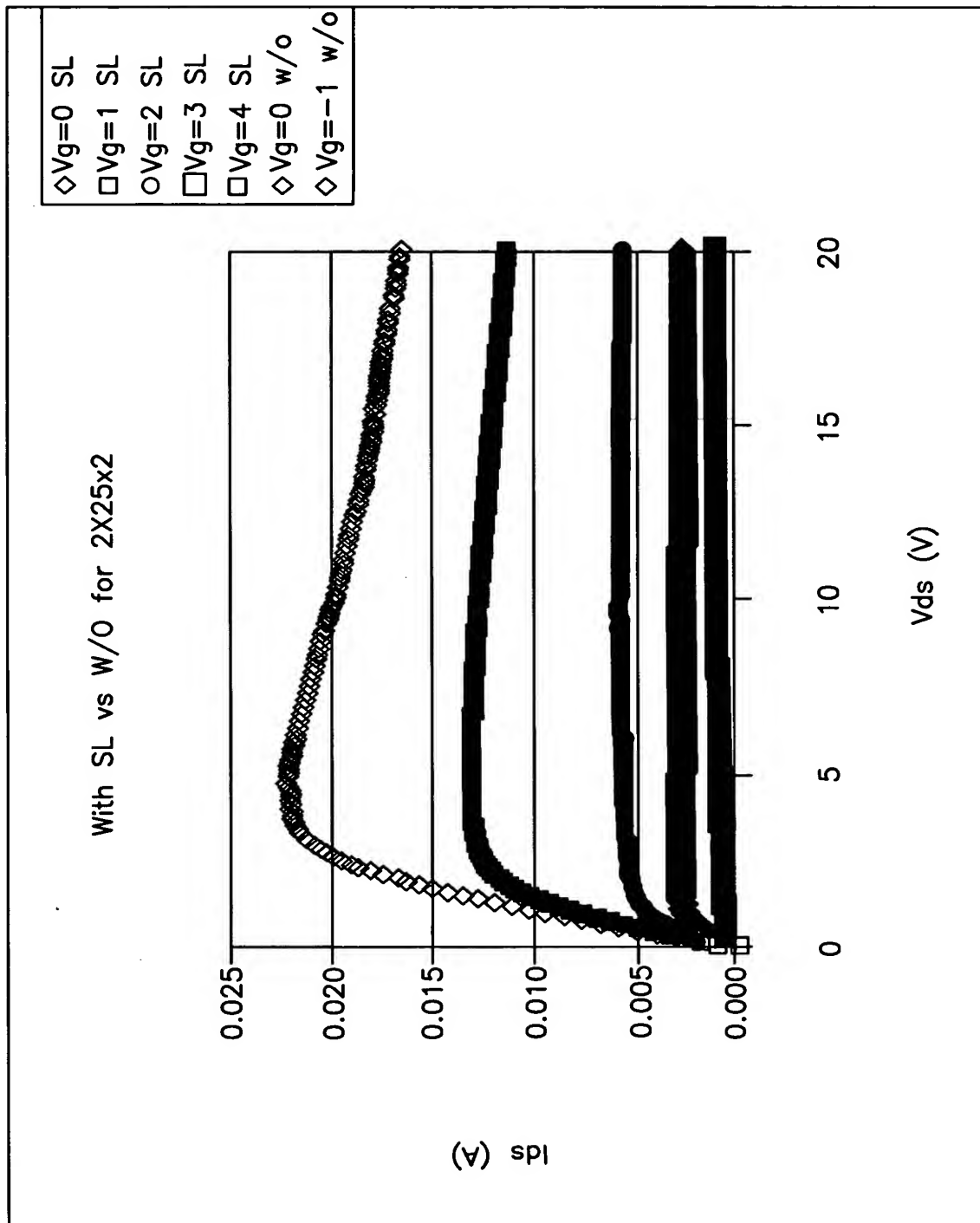


FIG. 11

